ESA supported Chip and ASIC Technology Developments for Exploration Missions including Planetary Probes

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Needs for and Advantages of Miniaturization (1)

Space missions, in particular planetary missions and planetary probes …

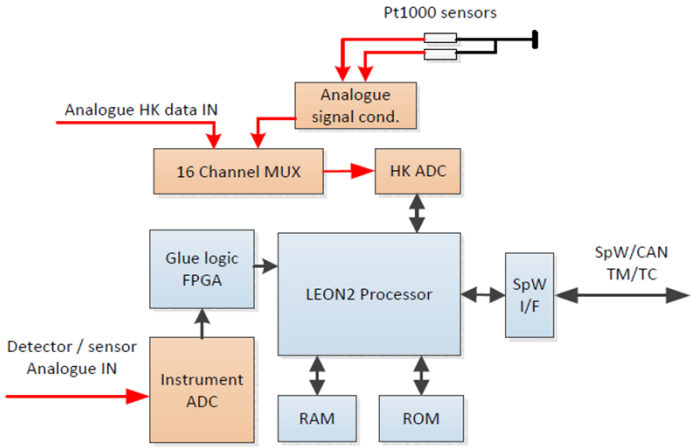
- Need a high delta V to reach their destination => launcher/cruise stage/spacecraft/ support system mass is ~proportional to payload & subsystem mass and rises ~exponentially with needed delta V
- Need power efficient systems – in particular for solar powered spacecraft the power system mass is ~proportional to energy consumption and panel mass rises with square of distance from the sun

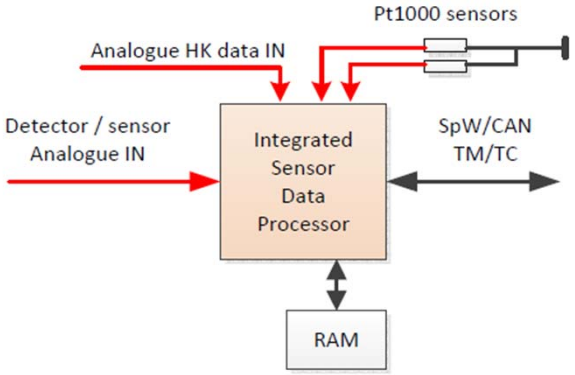
Miniaturization / higher degree of electronics integration provide …

- Reduced size and mass of electronics
- Reduced power consumption
- Higher reliability in comparison to systems based on discrete components
- In many cases, higher performances (processing power, bandwidth, functionality)
- Cost reductions if economies of scale can be achieved

Needs for and Advantages of Miniaturization (2)

Example: integration of a typical instrument digital electronics design





Traditional design:

- GPP, FPGA, ADC, RAM, ROM, extra HK DAQ H/W
- Min 5 digital ICs
- Min 3 analogue ICs
- Some discrete analogue circuitry
- Ca 100 cm^2 ?
- 5-8 Watts ?

⇒ **Ca 50-70% power savings**
⇒ **Ca 60-70% mass and volume savings**
⇒ **Higher reliability**

Integrated design:

- Mixed signal ASIC
- RAM only, programmed via SpW RMAP
- Direct support for standard HK sensors
- Reduced analogue circuitry
- Ca 30-40 cm^2 ?
- 2-3 Watts ?

Power consumption

Power consumption

The power consumption of a spacecraft element has impacts along the power supply chain:

Power / energy impact:

Unit power consumption
+ Converter losses (~30%)
+ Battery discharge losses (some %)
+ Battery charge losses (some %)
+ Harness & other losses
= power required from solar panels

Mass impact:

Δ Converter mass
Δ battery mass
Δ regulator mass
Δ structural mass
Δ solar panel mass

System level mass impact of power consumption increase

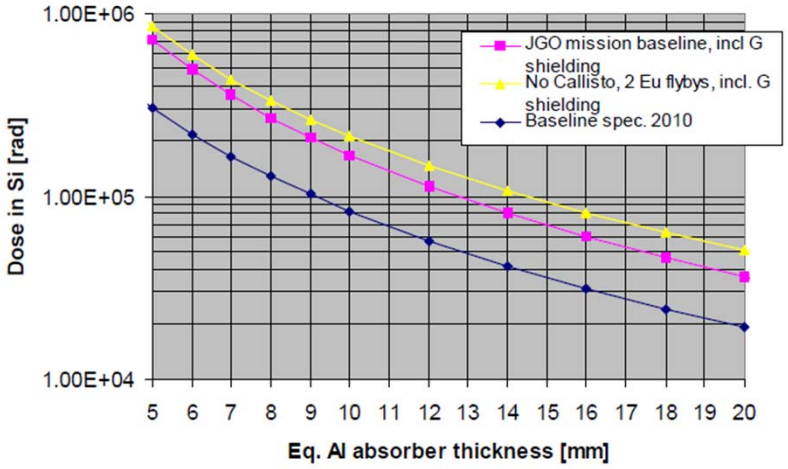
	EO Example	Mars Orbiter Example	Mars rover Example	Jupiter orbiter Camera Example
Power / delta power [W]	1.000	1.000	1.000	1.000
Power conditioning electronics mass impact [kg/Watt]	0.030	0.030	0.030	0.030
Power conditioning mass / delta mass [kg]	0.030	0.030	0.030	0.030
Power condintioning efficiency [%]	70.000	70.000	70.000	70.000
Power needed from battery [Watts]	1.429	1.429	1.429	1.429
Battery capacity [Wh/kg]	150.000	150.000	150.000	150.000
Demand cycle (ops cycle) duration [hours]	1.500	8.000	12.000	24.000
Power / delta power storage demand duration [hours]	0.750	2.000	6.000	2.000
Battery charge / discharge efficiency [%]	90.000	90.000	90.000	90.000
Battery mass / delta mass [kg]	0.007	0.019	0.057	0.019
Energy needed from solar panel {Watt-hours]	2.381	12.698	19.048	38.095
Solar power generation constant [W/m^2]	200.000	86.000	65.000	7.500
Earth = 200 W/m^2, Mars = 86 W/m^2, Jupiter 7.5 W/m^2				
Solar power generation duration per OPS cycle [hrs]	0.750	6.000	4.000	22.000
Solar panel power / delta power needed [Watts]	3.175	2.116	4.762	1.732
Solar panel mass per area [kg/m^2]	4.500	4.500	8.500	4.500
4.5 kg/m^2 for deployed / 2.25 kg/m^2 for body fixed panels				
deployable panels 4.5 Watt/kg, fixed panels 10 Watt/kg (?)				
Solar Panel area needed [m^2]	0.016	0.025	0.073	0.231
Solar panel mass / delta mass [kg]	0.071	0.111	0.623	1.039
Thermal subsystem mass increase [kg/Watt]	0.020	0.020	0.020	0.020
Thermal subsystem mass / delta mass [kg]	0.029	0.029	0.029	0.029
Total mass / delta mass * [kg]	0.137	0.188	0.738	1.117
* on the vehicle; impact on structure & harness neglected.				

⇒ For solar powered S/C mass impact of power consumption strongly depends on solar distance
⇒ Impact moderate at Earth distance, but very high at Jupiter distance
⇒ Power efficiency is essential in outer solar system in particular if S/C is solar powered
⇒ Note: for similar IC technology, ASICs are 2-4 times more power efficient than FPGAs

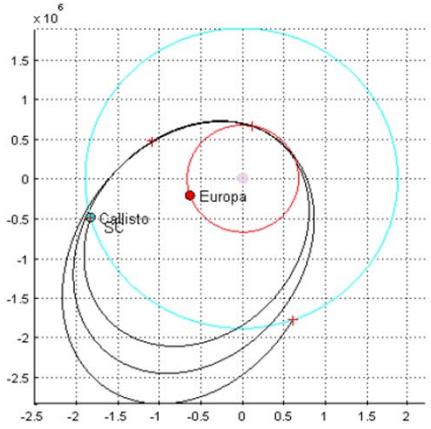
Radiation hardness

.. is a key requirement for reliable space electronics. Total dose (TID) and Single Effect Event (SEE) related requirements vary from mission to mission

1. Increase of modelled radiation exposure (2x wrt previous baseline)
2. Inclusion of Europa flybys (adds ~20% to total dose)



Courtesy C. Erd, SRE, ESA/ESTEC



Example: JUICE Jupiter mission candidate trajectory

⇒ **For demanding missions, low radiation hardness of components requires significant mass investments for shielding**

⇒ **Suitable ASIC technologies can reduce shielding mass and be an enabling technology in specific areas**

High TRL ASIC libraries available in Europe

Available / established Digital ASIC Technology

- ATMEL 180nm, ESCC qualified, 300 krad, TRL 9 today

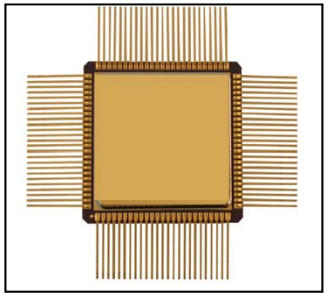
DARE (Design Against Radiation Effects) technology

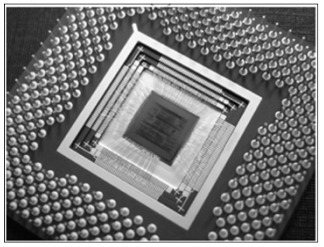
- 180nm, mixed signal, 1Mrad, library developed by IMEC (BE)
- Commercial (non-space) foundry used for die production
- Further development contract started 2011
- Flight chips have been produced , TRL 9 expected ~2013

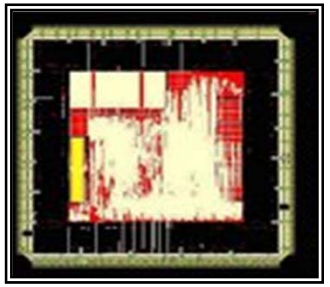
Future digital ASIC technology

- DSM technology developed by ST microelectronics
- 65 nm, up to 400 MHz, up to 30 Mgates
- High speed serial links (goal 6.25 Gbit/sec)
- Under development, TRL 9 expected ~2015

Mixed signal is key for high integration in science / instrumentation applications







The DARE libraries

DARE (Design Against Radiation Effects) Libraries:

Radiation-hardened-by-design libraries in standard commercial technology, developed / advanced in ESA contracts, available at *imec* (BE)

- DARE180 well supported (UMC .18)
- DARE90 small core & IO library available, development needs to be continued to extend library (UMC 90nm)
- I3T80RH kit

Manufacturing, Packaging, Testing, Characterization (lot) Qualification & Radiation test up to FM is supported by imec's ASIC Services

- Through subcontractors (Microtest, Maser, MAPRAD, others)

Flexible solution

- DARE allows for mixed signal design
  - Can add specific analog blocks; designed by customer, design house or imec
- Cells can be added to the library
- IO pads can be customized ...

The DARE libraries – DARE180

		Logic	RF	CIS
Core 1.8V	combinatorial	50	🛠	50
	normal' FF's	20	🛠	20
	HIT FF's	20	🛠	20
	HIT FF with M1 progr. Reset	no	no	4
	Clock Gating cells	🛠	🛠	4
	TIEx	2	🛠	2
IO	Digital IO 70x70	40	no	no
	Digital IO 110x110	40	🛠	40
IO	Analog IO 70x70 Any	5	no	no
	Analog IO 110x110	5	🛠	6
IO	LVDS 70x70 Any	3	no	no
	LVDS 110x110	3	🛠	3
IO	PLL 70x70	1	no	no
	PLL 110x110	1	🛠	1
SRAM Compiler (6Tor cell)		🛠	no	no

IO at 3.3 and 2.5 V

ESD Optimization 🛠

Extended Common Mode Range 🛠

SEE update 🛠

DPRAM Compiler 🛠

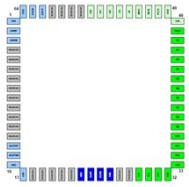
Low-speed ADC
Low-speed DAC

Voltage regulator 🛠

+ Customer Requests
+ Additional Analog IP developed by an external design house (fast DAC, ADC, ...)

Components and Chip prototypes (1)

"Frontend Read-out ASIC for Cosmic Vision Instrumentation Payload"



Contractor: Arquimea, Spain

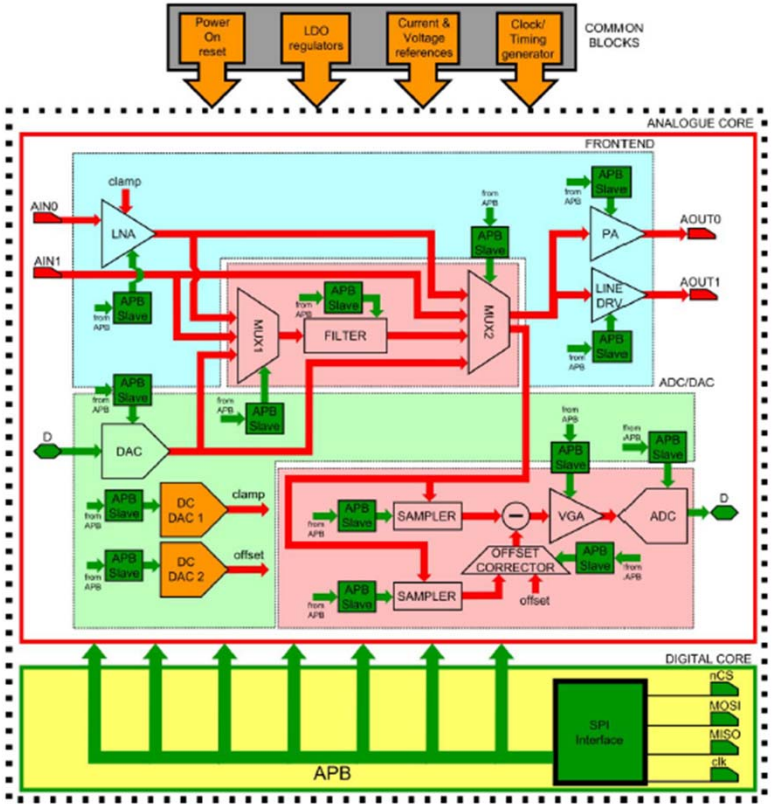
Minimum specs:

- -55 to 125 deg C
- 300 Krad TID
- 100 FIT
- 64 pin ceramic pkg
- 3.3 Volt supply
- ca. 1W max
- Parallel 16 bit I/F
- SPI bus
- ADC 19bit * 100 kHz /
  16 bit @ 1 MHz /
  14 bit @ 10 MHz,
  2 Vpp input
- DAC same resolution,
  2 Vpp output

- Chip configurations:

- CCD signal processor
- Radiation detector
- Radiation spectrometer
- ADC DAC
- Filter
- Low noise amplifier
- Power amplifier

Prototypes expected
Early 2013



Components and Chip prototypes (2)

“Configurable Mixed Signal ASIC for Cosmic Vision Instrumentation Payload”

=> Functionality similar to frontend ASIC but faster / different internal design

Contractor: Arquimea, Spain

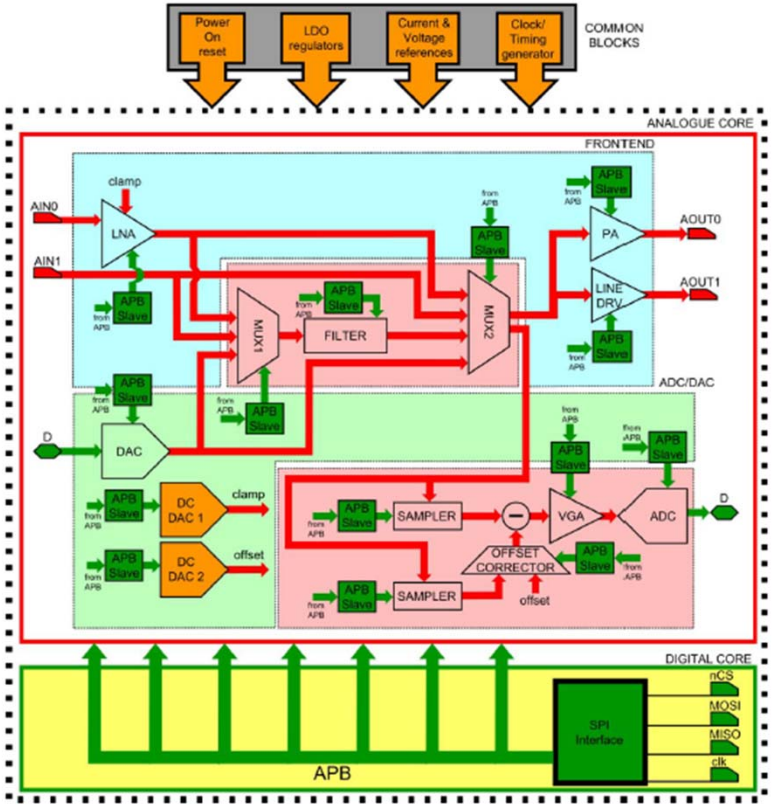
Minimum specs:

- -55 to 125 deg C
- 300 Krad TID
- 100 FIT
- 64 pin ceramic pkg
- 3.3 Volt supply
- ca. 1W max
- Parallel 16 bit I/F
- SPI bus
- ADC 15bit @ 100 MHz / (ENOB 12 bits)
- 2 Vpp input
- DAC same resolution, 2 Vpp output

- Chip configurations:

- CCD signal processor
- Radiation detector
- Radiation spectrometer
- ADC DAC
- Filter
- Low noise amplifier
- Power amplifier

Prototypes expected Early 2013

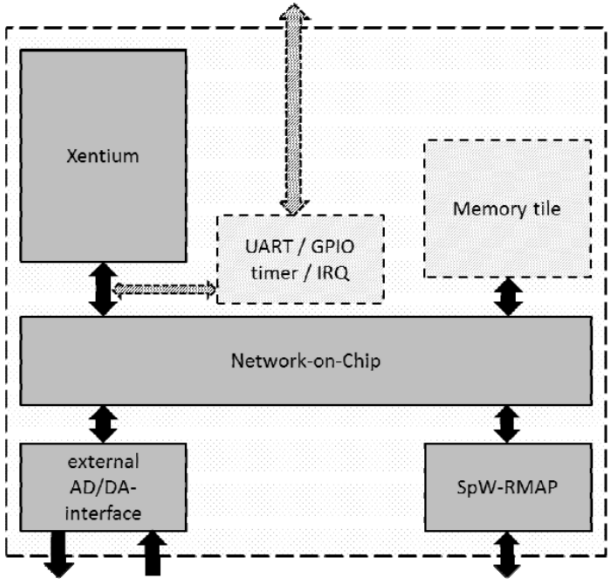


Components and Chip prototypes (3)

DARE+ Application ASIC: DSP, NoC, bridges and interfaces

Contractor: IMEC (BE) and RECORE b.v. (NL)

- Xentium ® fixed-point DSP @ ca 100 MHz
- NoC (Network on Chip) routers and bridges
- NoC connected SpW with RMAP support
- NoC connected Memory Tile
- bridge to external ADC (STM RH1401)*
- bridge to external DAC (ADI AD768)*
- UART/I2C/SPI interface to external chips



IP developed by RECORE b.v., NL

<u>Other useful prototyping:</u>

- analogue multiplexer elements

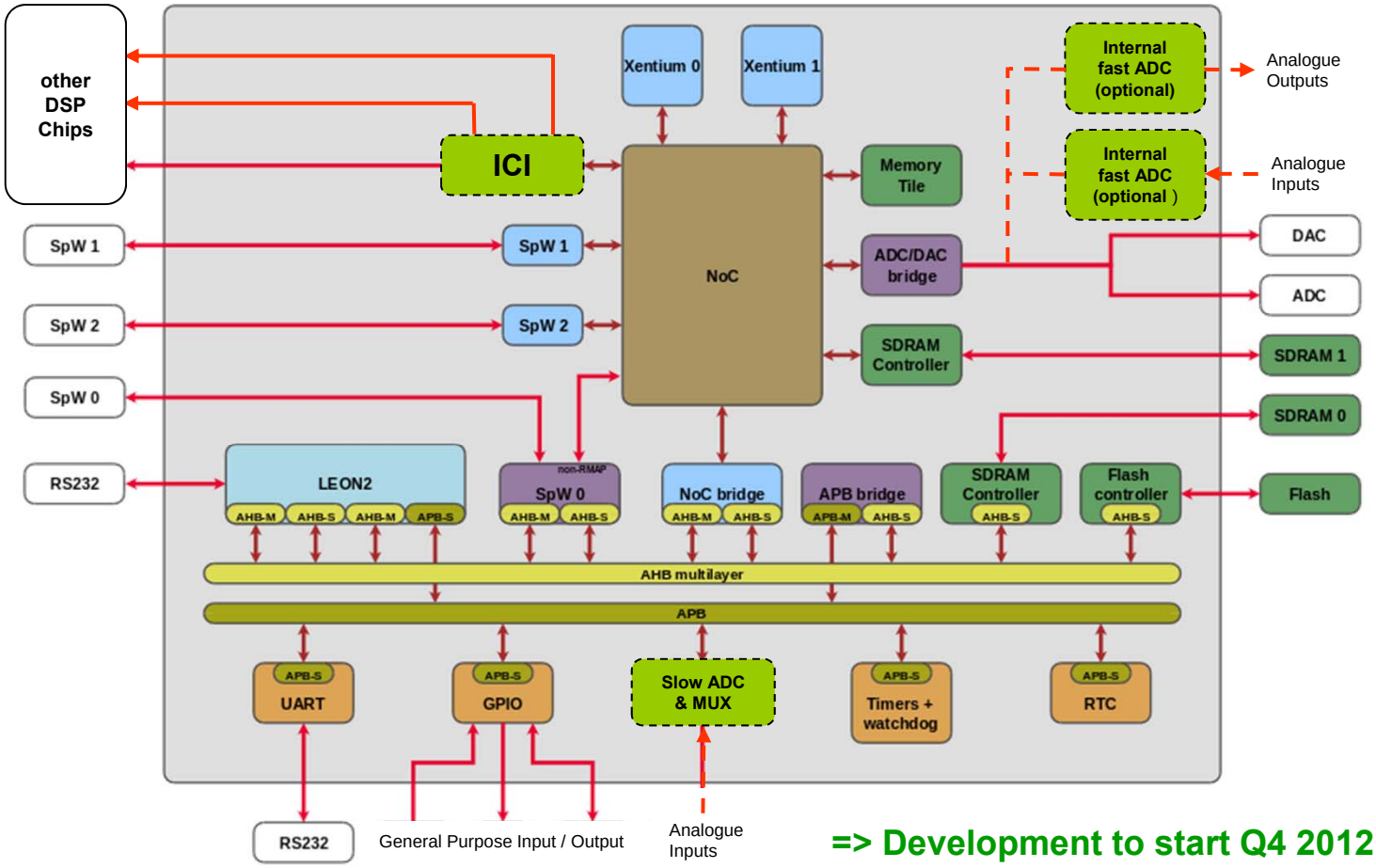
=> Hardened IP will be available for licensing

=> Prototypes expected Q1 2013

***interface compatibility to aforementioned frontend & configurable ASIC developments**

Envisaged chip developments

Based on the ongoing DARE+ development / prototyping activity new ASIC developments can be initiated: data processor chip for exploration missions



Proposed Features:

- LEON GPP
- 2 VLIW DSPs
- HK ADC
- HK MUX
- On-chip memory tile
- Rad-hardened, 1 Mrad
- On-chip science ADC (optional)
- On-chip DAC (optional)
- PWM outputs
- SpW links
- Parallel I/O
- Ext. ADC/DAC bridges
- Support for HK data sensors

=> Development to start Q4 2012 if funding is confirmed

ASIC cost vs. OTS component cost

Example cost comparison: Available space qualified components vs. new mixed signal chip development for a planetary orbiter strawman payload set

Planetary orbiter - strawman payload
FPGAs or ASICs for digital data processing & HK

Name	expected FPGA / ASIC need (set)	# EMs sets	# FMs sets	Estimated part cost in Euro: 2 chip sets for E(Q)M + 1 spare cost EMs set	3 chip sets for FMs + 1 spare cost FMs set	Total cost instrument
Radiometer	standard LEON (calculated) or dedicated ASIC	2	3	5000	20000	70000
Dust Sensor	assumed virtex-5 (calculated) , or dedicated ASIC	2	3	1000	70000	212000
Imaging spectrometer	LEON plus RTAX2000, or dedicated ASIC	2	3	12000	50000	174000
IR spectrometer	assumed virtex-5 (calculated) , or dedicated ASIC	2	3	1000	70000	212000
Plasma Package	DPU: 2 Virtex 4+RTAX4000 (=LEON); boards with 3 VIRTEX 4; DCDC board RTAX2000, or dedicated ASIC plus small FPGAs	2	3	75000	230000	840000
Magnetometer	DPU: LEON3, 3 sensor boards with RTAX2000S, or dedicated DARE based chips possibly with smaller FPGAs	2	3	20000	80000	280000
Plasma Instrument	RTAX 4000 assumed	2	3	7500	30000	105000
Wide angle camera	LEON+FPGA meets requirements (assumed: LEON2 + RTAX 2000) or dedicated ASIC	2	3	10000	40000	140000
Hi Res Camera	LEON+FPGA meets requirements (assumed: LEON2 + RTAX 2000) or dedicated ASIC	2	3	10000	40000	140000
Imager	LEON+FPGA meets requirements (assumed: LEON2 + RTAX 2000) or dedicated ASIC	2	3	10000	40000	140000
	Total estimated cost - digital components					**~2300k**
	Additional analogue components (HK ADC, MUX, signal cond)					**est. ~700k**

ROM result:

⇒ **For the assessed strawman payload ca 3 M€ are required for digital data processing chips (uP, FPGA, HK DAQ)**

⇒ **A dedicated ASIC development & qualification has similar cost**

⇒ **Not feasible for individual payloads (cost too high)**

⇒ **To be considered for projects**

⇒ **Considering re-use potential, should be attractive to Agencies & Primes**

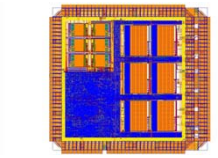
DARE future evolution

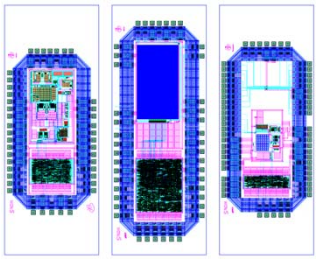
ASIC Libraries are evolving, and # of available cells / IOs / IPs is growing

DARE180:

ESA funded DARE+ activity (completion 2013) ongoing

- correction of memory compilers
- New library elements
- Demonstration of hardened fixed point VLIW DSP IP and NoC
- Frontend ASIC IPs - analogue and digital functions (ADC, DAC, filters, etc)

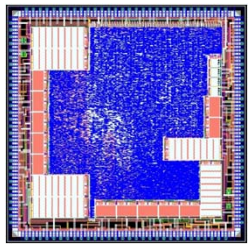




DARE 90:

Next step towards higher performance mixed-signal ASICs

- Core (digital) library available
- New elements, analogue IPs etc need to be developed
- Needs and available funding determine schedule



Summary / Conclusions

Miniaturization and further electronics integration are key for future missions

- Reduced mass & power, increased reliability, higher performances can be achieved

Power consumption and radiation hardness are often critical parameters

- TID for S/C in harsh environments, power in particular for outer solar system missions

Both digital and mixed signal libraries are available in Europe for new ASIC developments

- Established 180nm, new mixed signal DARE180 and future STM 65nm and DARE90
- A range of mixed signal IP (converters, MUX, PLL, others) become available for DARE180

Several new components are under development on DARE180

- Analogue frontend / converter components are foreseen for qualification
- Prototyped and validated IPs will be available /licensable for system on chip developments
- New mixed signal data processor chip development for exploration missions likely to start soon

ASIC developments can be economic for small to medium numbers of chips

- Difficult for single system developments but can be very attractive already for moderate numbers

Libraries will evolve and IP pool is expected to grow

- More IP becoming available to users, 90nm DARE / possibly other libraries to follow