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University of Idaho
College of Engineering

Development of Smaller Power Technologies For Use in Planetary Probes

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American Semiconductor Inc.

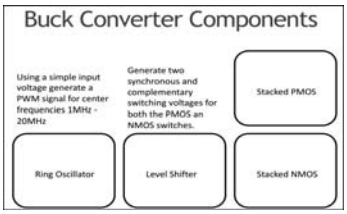
Abstract

Power conversion is essential to any circuit on board a planetary probe. The University of Idaho Integrated Passives Research Team has been developing high voltage performance power converters on chip in low voltage fabrication processes to improve power conversion. The Integrated Passives team creates the chips and power circuits, whereas Dr. Choi of the Materials Science Department at UI along with Dr. Hong has created the inductors and capacitors that are post processed on the chip using nanoscale fabrication methods. This results in the creation of more improved power converters on chip. These power converters are able to interface lightly regulated, high voltage DC inputs into regulated DC outputs for use on chip. The chips are designed with both bulk CMOS and Silicon on Insulator (SOI), radiation hardened and not. Those power converters that are designed with SOI radiation hardened processes are given a clear advantage over bulk CMOS circuits. The SOI process creates better voltage isolation which in turn improves high voltage performance, bandwidth and temperature characteristics and also gives better temperature and radiation performance than similar bulk CMOS circuitry. They are readily laid out and can handle about ten times the input voltage rating of the process. The results of this research are more efficient power supplies that are smaller, lighter and closer to the load. These supplies are almost always contained within the same package and in many cases placed on the same chip, saving space and allowing for more components in the circuit. This work has significant advantages for planetary probes which must either be contained within a tightly spaced environmentally controlled area or, in some cases such as SOI versions, they can survive more radiation and temperature extremes.

Background

The Integrated Passives Team has been working on ultra low power CMOS electronics at the Uofl for the past several years. Historically, our process voltage target was 5V. Over time, we went to 3.3V to 2.5V and are currently at 1.8V.

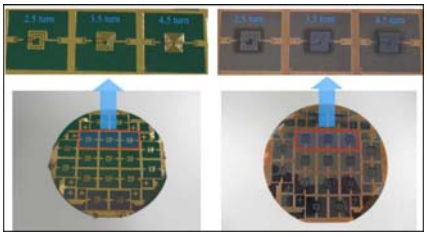
This output is achieved through a Buck Converter and the pieces of this converter are shown below. The chart describes the size of the current SOI Flexfet technology of American Semiconductor Inc. and compares it with the process of the previous chip design, showing decreased input voltage and increased output voltage at a smaller process (180nm).

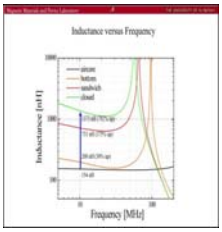


	250nm Flexfet FD SOI	180nm Flexfet FD SOI
Frequency	1MHz	20MHz
Duty Cycle	50%	50%
Input Voltage	5V	3.3V
Output Voltage	.9V	1.2V
Desired Output	3.5V	1.65V
Voltage Drop	2.6	0.45V
Avg. Current	15mA	25mA

Inductors

Air-Core Inductor **Magnetic-Core Inductor**





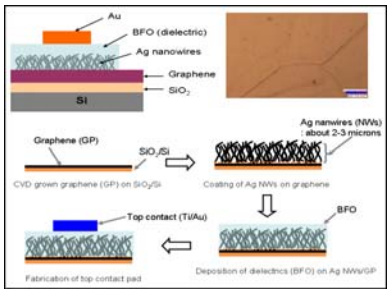
Dr. Hong from the University of Alabama developed these inductors, which the Int. Passives Team uses. The Inductors should be fabricated at the "back end" of the process, but:

- Sputtering ferrites is a high-temperature operation (1500C)
  - Would melt CMOS aluminum interconnects (600C)
- Yang-ki Hong from University of Alabama has also developed an Electrophoresis Deposition (EPD) method that works at room temperature
- You Qiang (UI Physics) has developed another low-temperature way to make ferrites.
  1. Accelerate nano-particles onto a target
  2. Build a film like snowballs against a wall
  3. Can control resistivity with controlled oxidation

Capacitors

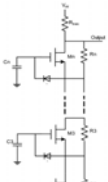
The capacitors shown are the 2nd generation of capacitors created by Dr. Choi's materials science group.

- Improved capacitance with Ag nanowires
  - Higher surface area
  - Higher conductivity
- Improved capacitance with Graphene as bottom contacts
  - Higher conductivity
  - Easy to incorporate with future graphene-based nanoelectronics



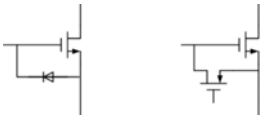
Stacked MOSFET Transistors

- The stacked MOSFET transistor is the basis for the converter's high input voltage tolerance.
- As M1 turns on, the source of M2 is pulled to ground.
- In the off state, C2 is charged through the resistor voltage divider to 1 Vdd/n-Vdiode, if the input voltage is some multiple of the process voltage.
- As the source of M2 is pulled down, a Vgs voltage is developed and M2 begins to turn on etc.



Diode-less Rectifiers

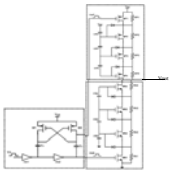
- Newest process does not allow fabrication of diodes
- Process restrictions are an important part of any design; this is a really big one that must be overcome here
- We replace the diode with a MOSFET
- This is called a Pass Gate; it works as a switch
- It is a method used in high performance power supplies



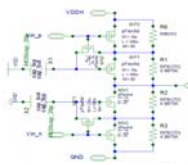
Stacked Buck Converter: Simulation Results

Stacked Buck Converter

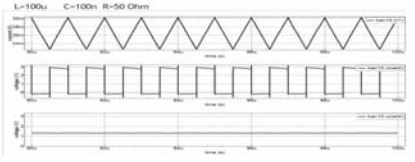
- Bidirectional converter
- Pass gate rectifiers
- Level shifter for coordinated switching



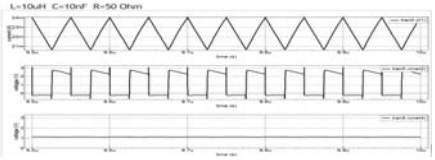
Stacked Buck Schematic



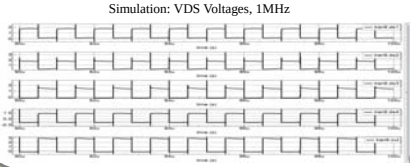
Simulation: Load, 1MHz



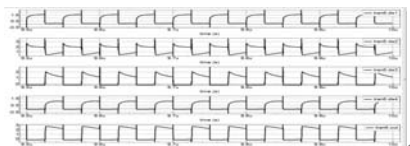
Simulation: Load, 20MHz



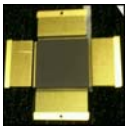
Simulation: VDS Voltages, 1MHz



Simulation: VDS Voltages, 20MHz



Summary



Current Chip Design

Planetary Probe

The Integrated Passives Team has developed a high voltage performance Buck Converter on chip in low voltage fabrication processes applicable for use in a planetary probe. We have switching semiconductor devices such as the LDMOSFET that give greater voltage capacity while keeping the performance advantages of SOI radiation hardened technology. We use a Pass Gate topology to address the lack of acceptable diodes in our digital circuit fabrication process. The stacked transistor topologies allow for a reliable, high voltage capability on a low voltage chip. We currently have high permeability cores with an enclosed topology that give higher inductance and greater Q values. The on-chip capacitors developed are 1-70nF/ mm^2. The SOI radiation hardened process and low voltage high performance is ideal for power conversion in a planetary probe, conserving overall energy and space requirements.